

REMARKS

Examiner Su Kim is thanked for the thorough examination and search of the subject Patent Application and for finding acceptable the corrected drawings and Specification.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of the rejection under 35 U.S.C. 102 of Claims 8, 16, 24, 26, and 27 as being anticipated by Matsuo is requested in accordance with the following remarks.

Claim 8 reads as follows:

8. A method for fabricating a CMOS semiconductor device structure comprising:
 - providing a dielectric layer on a substrate;
 - depositing a hafnium nitride layer overlying said dielectric layer;
 - depositing a capping layer overlying said hafnium nitride layer;
 - patterning said hafnium nitride layer and said capping layer and said dielectric layer to form CMOS gate electrodes; and
 - forming source and drain regions within said substrate adjacent to said CMOS gate electrodes.

Applicants claim formation of CMOS gate electrodes by depositing a hafnium nitride layer over a dielectric layer, depositing a capping layer over the hafnium nitride layer, then patterning the gate stack comprising the hafnium nitride layer, the capping layer, and the dielectric layer to form CMOS gate electrodes. . It is agreed that Matsuo deposits hafnium nitride using CVD over a dielectric layer (paragraphs 0014 and 0015). However, next Matsuo removes the hafnium nitride “from the p-type region alone.” (paragraph 0018). This etching step does not remove the underlying dielectric layer and no “capping layer” exists at this point in

Matsuo. In paragraph 0019, a tantalum nitride layer is deposited in both the NMOS and PMOS areas, but the HfN has been removed in the PMOS area prior to this deposition. Next, an aluminum layer is deposited to complete the CMISFET (paragraphs 0020 and 0021). Note that this entire process is a damascene process rather than a patterning process as in Applicants' invention. This is clearly different from Applicants' invention. Applicants' patterning of the capping layer, hafnium nitride layer, and dielectric layer to form the CMOS gate electrodes is not taught by Matsuo. The only patterning done by Matsuo is to remove the hafnium nitride layer in the PMOS region.

Claim 16 reads as follows:

16. A method for fabricating a CMOS semiconductor device structure comprising:
providing a dielectric layer on a substrate;
depositing a first metal layer overlying said dielectric layer;
patterning said first metal layer and said dielectric layer to form CMOS gate electrodes;
and
forming source and drain regions within said substrate adjacent to said CMOS gate electrodes.

Applicants claim formation of CMOS gate electrodes by depositing a first metal layer over a dielectric layer and patterning the gate stack comprising the first metal layer and the dielectric layer to form CMOS gate electrodes. It is agreed that Matsuo deposits hafnium nitride using CVD over a dielectric layer (paragraphs 0014 and 0015). However, next Matsuo removes the hafnium nitride "from the p-type region alone." This etching step does not remove the underlying dielectric layer (paragraph 0018). Furthermore, this etching step does not form the CMOS gate electrodes. Matsuo must further deposit a tantalum nitride layer and an aluminum layer to complete the CMISFET. Note further that the HfN has been removed in the PMOS area prior to this deposition. This is clearly different from Applicants' invention. Applicants'

patterning of the first metal layer and the dielectric layer to form the CMOS gate electrodes is not taught by Matsuo. The only patterning done by Matsuo is to remove the hafnium nitride layer in the PMOS region.

Claim 24 claims depositing a second metal capping layer overlying the first metal layer *prior to* the patterning step. Matsuo deposits the tantalum nitride layer *after* removing the hafnium nitride layer in the PMOS region. This is clearly a different order of steps than in Applicants' invention.

Reconsideration of the rejection under 35 U.S.C. 102 of Claims 8, 16, 24, 26, and 27 as being anticipated by Matsuo is requested in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 9 and 17 as being unpatentable over Matsuo and in view of Yu et al is requested in accordance with the following remarks.

It is agreed that the paper to Yu et al, co-authored by the Applicants, discloses depositing hafnium nitride in an Ar and N₂ ambient. Claims 9 and 17 provide details about the depositing step in the process claimed in claims 8 and 16. As discussed above, Applicants' patterning of the capping layer, hafnium nitride layer, and dielectric layer to form the CMOS gate electrodes, claimed in claims 8 and 16, is not taught by Matsuo. The only patterning done by Matsuo is to remove the hafnium nitride layer in the PMOS region.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 9 and 17 as being unpatentable over Matsuo and in view of Yu et al is requested in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 13 and 21 as being unpatentable over Matsuo and in view of Yu et al is requested in accordance with the following remarks.

Yu et al in column 2 of page 230 state a ratio of $H_2:N_2$ of 1:1. No mention is made here of varying the ratio. Toward the end of the paragraph in the second column of page 231, it is stated that the work function *may* depend on the HfN concentration and that this is under investigation. Applicants claim in claims 13 and 21 that the work function of the gate electrodes is adjusted by varying the atomic ratio of nitrogen to hafnium and further claim that the ratio must be greater than or equal to 1. Thus, while Yu et al suggests that the concentration of HfN may affect the work function, Applicants' invention confirms that the HfN concentration affects the work function and further provides parameters for the variation.

Furthermore, as discussed above, Applicants' patterning of the capping layer, hafnium nitride layer, and dielectric layer to form the CMOS gate electrodes, claimed in claims 8 and 16, is not taught by Matsuo.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 13 and 21 as being unpatentable over Matsuo and in view of Yu et al is requested in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 14 and 22 as being unpatentable over Matsuo and in view of Yu et al is requested in accordance with the following remarks.

Yu et al discloses an RTA oxidation of the HfN film surface. It is not agreed that this is an express disclosure of impurity doping of the HfN film. Furthermore, on page 231, column 2, it is noted that the work function slightly increases after this RTA. The increase is attributed to the change of HfN crystallization. This is no teaching or suggestion that the RTA is for the purpose of tuning the work function or even that the slight increase in work function is desired. Applicants claim in claims 14 and 22 that impurity doping into the hafnium nitride layer is for the purpose of tuning the work function of the gate electrodes.

Matsuo optimizes the work function of the gate electrode by using a hafnium nitride layer having a first work function in the n-type region and by using a graphic organic coating film having a second work function in both the n-type and p-type regions. There would be no reason to oxidize the hafnium nitride layer in the n-type region of Matsuo, even if the slight increase in work function were desired since Matsuo achieves different work functions by using different materials in the n-type and p-type regions. Furthermore, Applicants' invention uses the same

mid-gap work function for both n-type and p-type gate electrodes. This is not taught or suggested by Matsuo alone or in combination with Yu et al.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 14 and 22 as being unpatentable over Matsuo and in view of Yu et al is requested in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 25 as being unpatentable over Matsuo is requested in accordance with the following remarks.

In alternative processes of Applicants' invention, HfN is either the first metal or the second metal layer. As discussed above, Matsuo does not pattern the gate stack (including the metal layer and the dielectric layer) to form the gate electrodes and Matsuo uses HfN only for the NMOS gate electrodes and not for PMOS gate electrodes. Applicants' invention deposits the first and second metal layers over the dielectric layer and patterns the first and second metal and dielectric layer to form both the NMOS and PMOS gates in a CMOS semiconductor device. This is not taught or suggested by Matsuo.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 25 as being unpatentable over Matsuo is requested in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 10-12, 15, 18-20, and 23 as being unpatentable over Matsuo is requested in accordance with the following remarks.

The instant claims provide further details about the invention claimed in independent claims 8 and 16. As discussed above, Applicants' invention of depositing and patterning HfN as part of a gate stack to form both the NMOS and PMOS gates in a CMOS semiconductor device is not taught or suggested by Matsuo.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 10-12, 15, 18-20, and 23 as being unpatentable over Matsuo is requested in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 102 of Claims 35, 37, 40-42, and 48 as being anticipated by Matsuo is requested in accordance with the following remarks.

Applicants claim formation of CMOS gate electrodes by depositing a hafnium nitride layer over a dielectric layer, depositing a capping layer over the hafnium nitride layer, then patterning the gate stack comprising the hafnium nitride layer, the capping layer, and the dielectric layer to form CMOS gate electrodes. Claim 35 specifies the capping layer comprises titanium nitride or tungsten. Claim 40 claims a first metal layer and a second metal capping layer. It is agreed that Matsuo deposits hafnium nitride using CVD over a dielectric layer (paragraphs 0014 and 0015). However, next Matsuo removes the hafnium nitride "from the p-type region alone." (paragraph 0018). This etching step removes only the Hafnium nitride layer. This etching step does not remove the underlying dielectric layer and no "capping layer" exists at this point in Matsuo. In paragraph 0019, a tantalum nitride layer is deposited in both the NMOS and PMOS areas, but the HfN has been removed in the PMOS area prior to this deposition.

Next, an aluminum layer is deposited to complete the CMISFET (paragraphs 0020 and 0021). Note that this entire process is a damascene process rather than a patterning process as in Applicants' invention. This is clearly different from Applicants' invention. Applicants' patterning of the second metal capping layer, the first metal layer, and the dielectric layer to form the CMOS gate electrodes is not taught by Matsuo. The only patterning done by Matsuo is to remove the hafnium nitride layer in the PMOS region.

Reconsideration of the rejection under 35 U.S.C. 102 of Claims 35, 37, 40-42, and 48 as being anticipated by Matsuo is requested in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 36, 38, 39, 43-45, 47, and 49-52 as being unpatentable over Matsuo and in view of Yu et al is requested in accordance with the following remarks.

As discussed above, Applicants' patterning of the capping layer, hafnium nitride layer, and dielectric layer to form the CMOS gate electrodes, claimed in claims 35 and 40, is not taught by Matsuo.

The instant claims provide further details about Applicants' claimed process. While Yu et al discloses depositing hafnium nitride in an Ar and N₂ ambient, Applicants' detailed claimed process is not taught or suggested by Matsuo alone or in combination with Yu et al. As discussed above, Yu et al does not teach adjusting the ratio of hafnium to nitride to adjust the work function nor do they teach impurity doping for the purpose of tuning the work function.

Applicants' invention deposits the first and second metal layers over the dielectric layer and patterns the first and second metal and dielectric layer to form both the NMOS and PMOS gates in a CMOS semiconductor device. In Applicants' invention, either the first metal or the second metal layer can be hafnium nitride. In either case, the hafnium nitride forms a part of both the NMOS and the PMOS gates. This is not taught or suggested by Matsuo.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 36, 38, 39, 43-45, 47, and 49-52 as being unpatentable over Matsuo and in view of Yu et al is requested in accordance with the remarks above.

Allowance of all Claims is requested.

It is requested that should Examiner Kim not find that the Claims are now Allowable that the Examiner call the undersigned at 765 4530866 to overcome any problems preventing allowance.

Respectfully submitted,

A handwritten signature in cursive script, reading "Rosemary L. S. Pike".

Rosemary L. S. Pike. Reg # 39,332